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Short communication

A novel integration approach for combining the components to minimize a micro-fuel cell

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Abstract

This work employs porous silicon as a gas diffusion layer (GDL) in a micro-fuel cell. Pt catalyst is deposited on the surface of, and inside, the porous silicon by the physical vapor deposition (PVD) method, to improve the porous silicon conductivity. Porous silicon with Pt catalyst replaces traditional GDL, and the Pt metal that remains on the rib is used to form a micro-thermal sensor in a single lithographic process.

The GDL was replaced by porous silicon and used in a proton exchange membrane fuel cell (PEMFC). Wet etching is applied to a 500 μm thick layer of silicon to yield fuel channels with a depth of 450 μm and a width of 200 μm. The pores in the fabricated structure had two diameters, 10 μm and less than 1 μm; its thickness was 50 μm. Accordingly, the GDLs of the fuel cell are fabricated using macro-porous silicon technology. Porous silicon was fabricated by photoelectrochemical porous silicon etching. The topside of the fuel channel was exposed to light from a halogen lamp. The porous structure was fabricated at the bottom of the fuel channel and patterned by anodization. The principles on which the method is based, the details of the fabrication flows, the set-up and the experimental results are all presented.

Keywords: Porous silicon; Photoelectrochemical; Anodization

1. Introduction

In recent years, the size of fuel cells has been minimized. They have been adopted in portable electronic products, such as cellular phones and PDAs. Silicon-based substrate is very compatible with micro-electro-mechanical-systems (MEMS) technology, and can be used to make chip-sized fuel cells. Hence, several investigations have attempted to reduce performed to reduce the total size of fuel cells; recent studies [1–3] are examples. The development of silicon-based substrate fuel cells has led to the use of fuel channels on silicon and then combined it with porous silicon. In fuel cells, porous silicon has been used as the gas diffusion layer to replace traditional carbon cloth or carbon paper [4,5]. It is also used to form proton exchange membranes [6].

Electrochemical etching in hydrofluoric acid has been studied since 1956. In 1990, Lehmann and Gösele [7] characterized porous silicon in detail. In 1996, Lehmann [8] examined the formation of an array porous silicon structure whose etching depends on electrolyte concentration, electrolyte temperature, silicon doping density and current density. Such structures are classified into three regimes by the average dimensions of the porous silicon. The microporous regime has mean dimensions of under 2 nm; the mesoporous has dimensions 2 nm to 50 nm, and the macroporous has dimensions of over 50 nm. Kleimann et al. [9] formed a macroporous array which was 42 μm wide and 200 μm deep. He showed that porous silicon etching technology could be applied to make a structure with a high aspect ratio structure at lower cost than associated with deep reactive ion etching (DRIE).

According to previous literature [10,11], several researchers have focused on measuring important data on the effect of cell temperature, fuel temperature, fuel humidity and other key factors on cell performance. Under the tendency, we will make the resistance temperature detector (RTD) sensor to integrate with the gas diffusion layer which is formed by anodization.

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2. Design and fabrication

Wet etching technology was utilized to form the fuel channels in a micro-fuel cell and then electrochemical etching was employed to make the gas diffusion layer from porous silicon. Therefore, in this study, the pore size and depth were controlled. The porous silicon structure was the macroporous regime and the macro- and mesopores had a limiting size of approximately. After the porous silicon was formed, the Pt metal was deposited on the pore surface as the catalyst of the fuel cell and the conductivity of the silicon was increased. Part of the Pt metal layer formed as the thermal sensor. Fig. 1 displays the design and fabrication flowchart.

2.1. Flow field design

Hoogers [12] shows the performance of the serpentine flow field on a fuel cell which was demonstrated to be better than the other flow field configurations (meshed and interdigitated) in some cases, because the fuel (gas or liquid) was pushed strongly to flow all around the active area of the fuel cell. Accordingly, the serpentine flow field was utilized in the design herein, as presented in Fig. 2. An N-type thickness of $525 \pm 25\,\mu m$, and a (1 0 0)-oriented double-side polished wafer was chosen. After the low pressure chemical vapor deposition (LPCVD) oxidation of Si_3N_4 on the silicon wafer (5000 Å thick), one side of the silicon was photolithographically processed. Reactive ion etching (RIE) was then applied transfer the pattern in Fig. 2, following the wet KOH etching process. This process is used to etch a silicon layer with a thickness of 450 μm. The remaining thickness of the silicon forms the gas diffusion layer, with a thickness of 50–70 μm, and a width of 200 μm. Fig. 3a–d showed the details of the process. After this process, the porous silicon is fabricated.

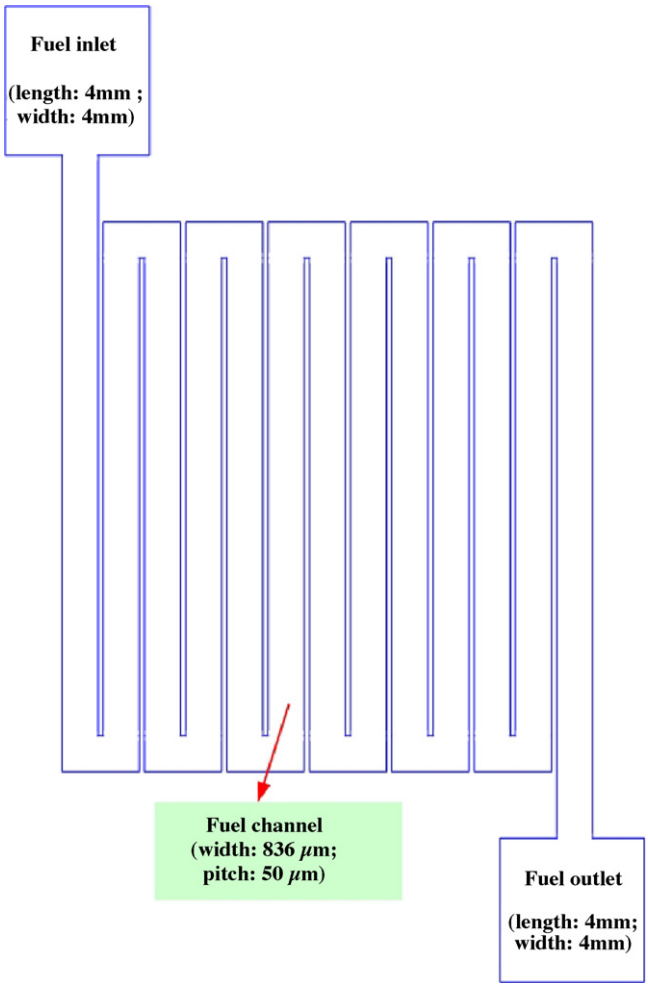

Fig. 2. Size and form of flow channel.

2.2. Fabrication of porous silicon

Porous silicon was electrochemically etched in HF electrolyte with an anodic bias applied to the silicon to form porous silicon on the side of the electrolyte. The applied anodic bias and the doping density strongly affect the pore size of the porous silicon. As stated above, N-type silicon with a resistivity of 1–20 Ω cm was employed, and the size of the porous silicon corresponded to the HF concentration and the etching current density. The approaches of other investigations [7,13] were used to design square pores of side 10 μm, and form fuel channels with vertical walls. The etching time and current density were the important parameters. In the proposed design, square pores of size 10 μm are fabricated by coherent porous silicon technology [7,13]. Coherent porous silicon technology can easily control the porosity and the pore diameter of the porous silicon could be easily controlled. The porous silicon was formed first using lithography to transfer the pattern, and then using electrochemical etching technology, as displayed in Fig. 4. The backside of the wafer was exposed to light from a halogen lamp, to generate the electron–hole pairs that drive silicon etching [14]. Fig. 3f–i presents the porous silicon fabrication process flow. After the flow field process was conducted as in Fig. 3a–e, the other side of the wafer was patterned lithographically, 10 μm square at a pitch of 15 μm covered the defined area, forming a gas diffusion layer 200 μm (Fig. 3f), then was transferred in the Si_3N_4. KOH wet etching on (1 0 0)-oriented silicon is anisotropic etching, and transforms 10 μm squares into inverted pyramids. Si_3N_4 was removed from the fuel field side of the wafer, after the fuel channel was formed. The side of the wafer was connected via an Al metal ring to the anode side of the power supply. These pyramidal etched pits concentrate the applied electric field and porous silicon etching begins at these tip locations, yielding perpendicular to the silicon surface (Fig. 3h). The electrolyte was

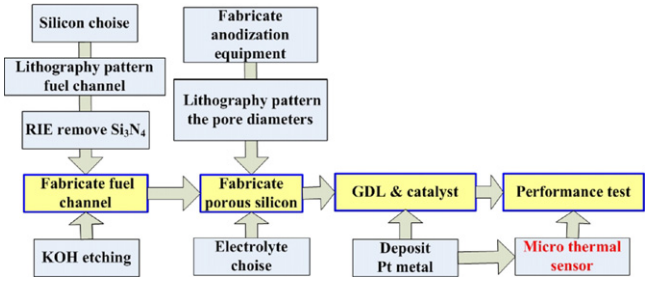

Fig. 1. Design and experimental flowchart.

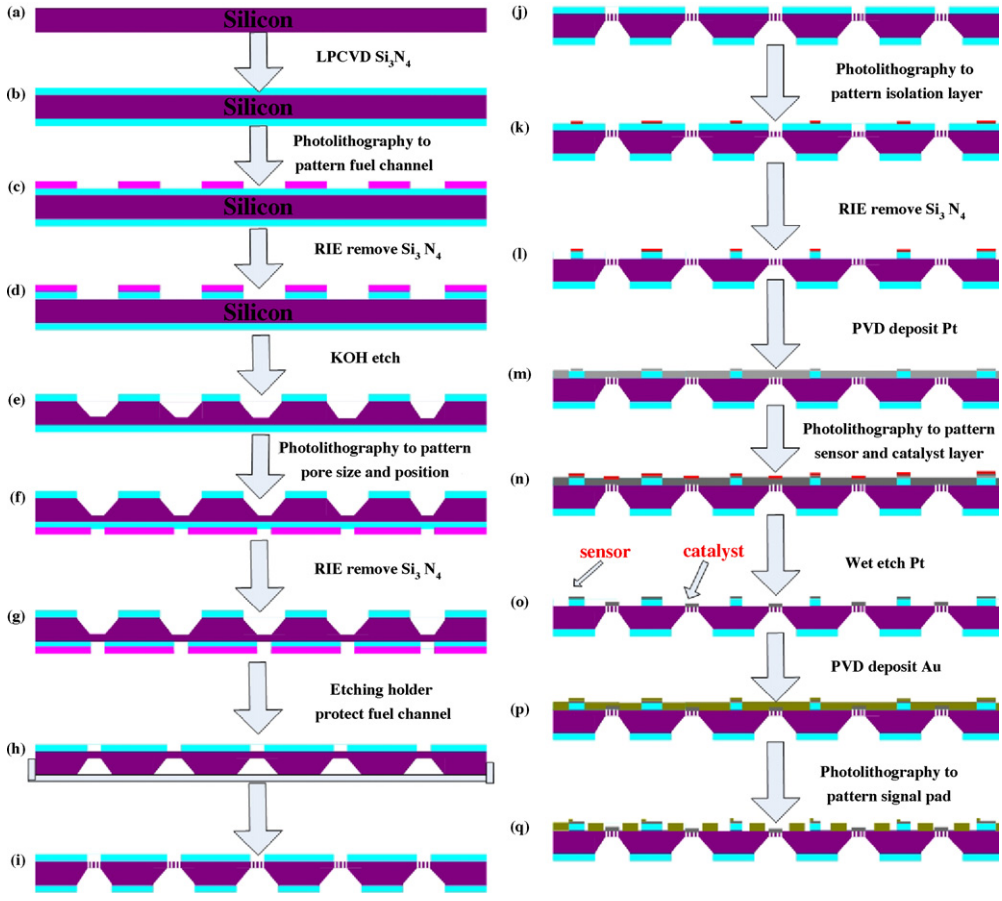

Fig. 3. Fabrication flowchart.

an HF-solution that was mixed with ethanol and water. To make sure the porous silicon through to flow field, we did not direct etching to reach the purpose. We used an equipment (Fig. 5) to protect the porous silicon already formed through KOH etching from having through-holes. If porous silicon technology was directly adopted to etch through-holes, the HF solution would leak out, which situation would be dangerous. Hence, the KOH solution must be prevented from etching the porous silicon, and the etch-back time must be controlled. Fig. 3i showed porous silicon through to flow filed. Another defined pore size was smaller than 1 μm, and the process flow differed from that associated with a diameter of 10 μm. A diameter of 10 μm was patterned by lithography technology on top of each flow channel. The pattern (200 μm × 13,140 μm) was transferred by Si_3N_4, and then produces the pore silicon using the etching equipment, as shown in Fig. 4.

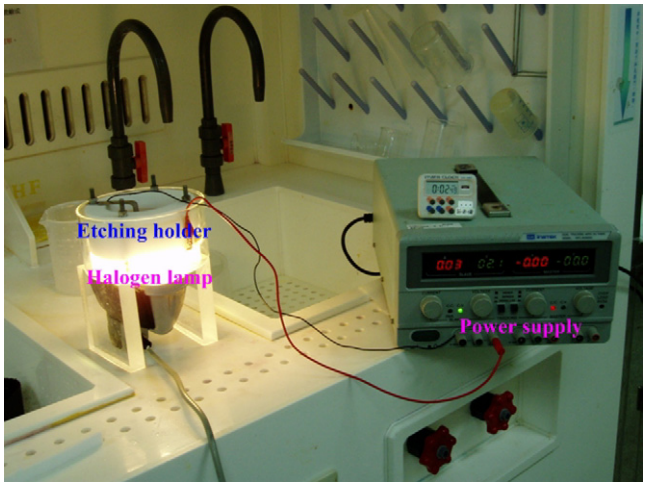

Fig. 4. Porous silicon etching equipment.

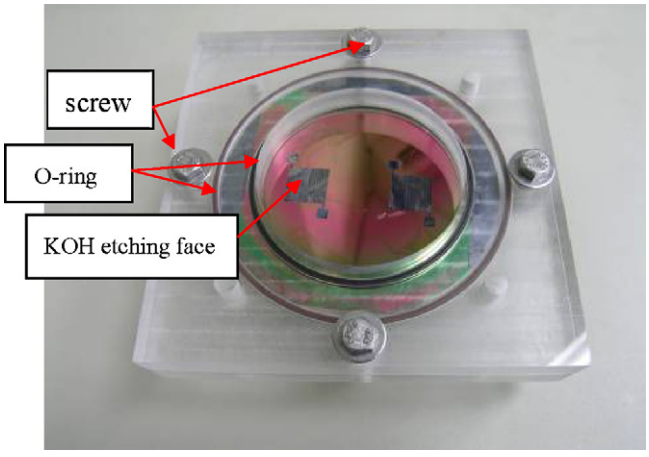

Fig. 5. Etching holder.

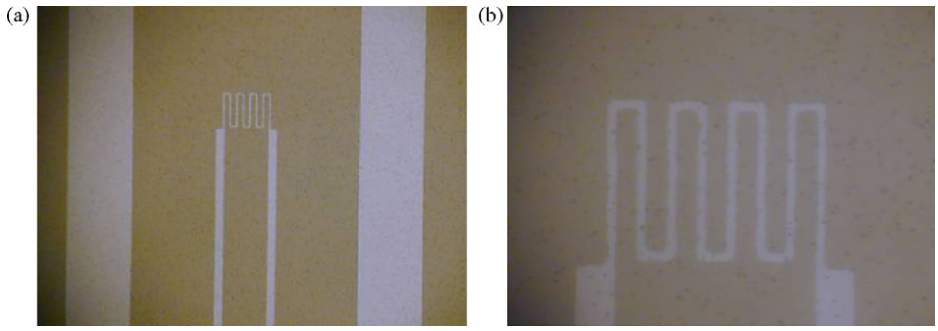

Fig. 6. Micro-thermal sensor pattern and microscopic photograph: (a) the overall vision and (b) enlarge the pattern.

2.3. Integrating catalyst and thermal sensor into gas diffusion layer

After the porous silicon was produced, the wafer was metallized on the porous silicon side with a layer of Ti/Pt (10 nm/100 nm). The Pt acted as the current collector and thermal sensor. Physical vapor deposition (PVD) was utilized to deposit Pt metal and wet etching was adopted to form the conductive layer and thermal sensors. Photoresist was employed as the etching mask, ensuring that the Pt metal remained on the surface of the porous silicon. The etching mask was used in lithography process by an exposing process. Fig. 3j–q display the process flow in detail. The micro-thermal sensor was fabricated, as presented in Fig. 6.

The experiment used temperatures of 20–46 °C. The resistance varied at 1.649–1.694 kΩ. Experimental results demonstrate that the temperature is almost linearly related to resistance, as shown in Fig. 7.

3. Results and discussions

In this investigation, two sizes of pores in silicon, 10 μm and less than 1 μm. The GDL of the fuel cell was replaced with 10 μm porous silicon. The 10 μm porous silicon was fabrication using 5%HF solution and the current density was 10 mA cm^{-2}, yielding an etching ratio of 1 μm min^{-1}. After 30 mins, a coherent pore size of 10 μm was obtained, as shown in Fig. 8. Other pore sizes in the porous silicon were formed using 50%HF solution and current density of 100 mA cm^{-2}, generating an etching ratio of 2 μm min^{-1}. It was etching silicon randomly. Therefore, the porosity and pore size were uncontrolled, as presented in Fig. 9. Accordingly, a fuel channel was combined in porous silicon. When a fuel channel formed, the 10 μm porous silicon, a through-hole, and it also has a conductive layer, as shown in Fig. 10. The Pt metal layer also formed the thin film thermal sensor on the ridge of the porous silicon side, as presented in Fig. 11.

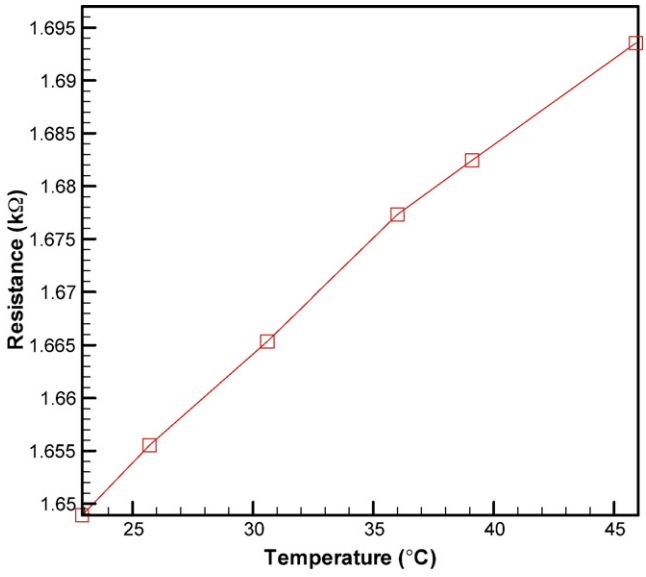

Fig. 7. The resistance vs. temperature curve.

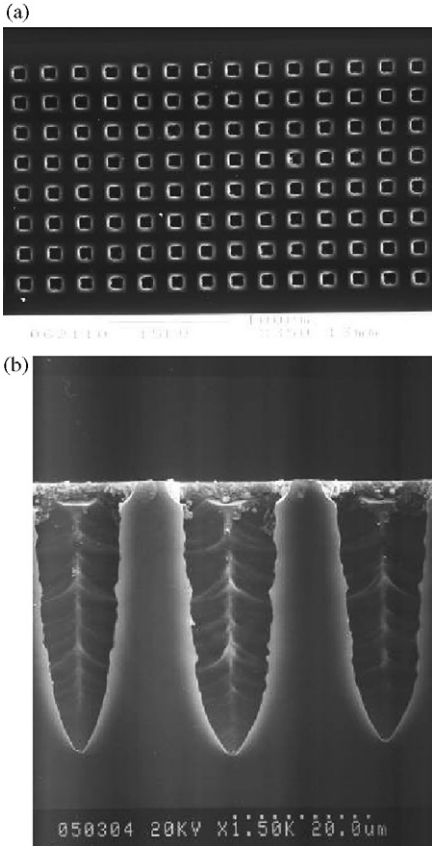

Fig. 8. SEM of the 10 μm porous silicon: (a) top view and (b) cross-section.

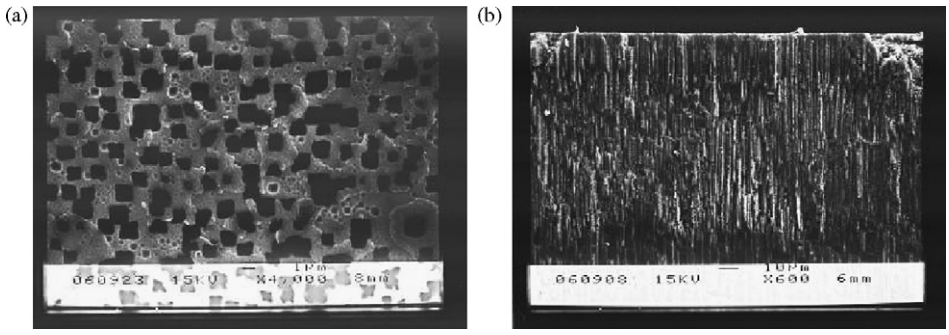

Fig. 9. SEM of under 1 μm porous silicon: (a) top view and (b) cross-section.

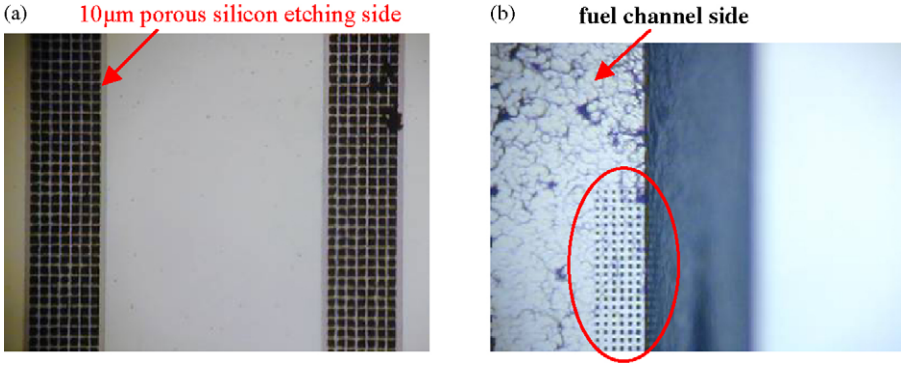

Fig. 10. Optical microscopic photograph of the porous silicon with fuel channel: (a) side of etched porous silicon and (b) red circle: fuel channel side seen through the porous silicon. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of the article.)

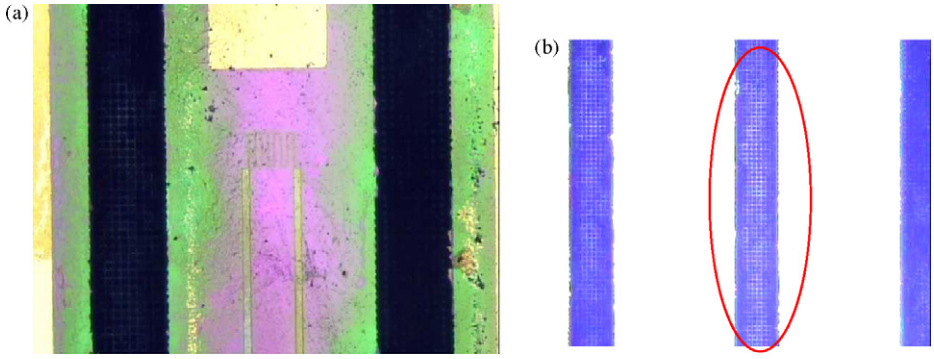

Fig. 11. Optical microscopic photograph of porous silicon combined with porous silicon structure: (a) sensor and porous silicon layer and (b) Pt catalyst (white spot) in a red circle by far sight and strongly light. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of the article.)

4. Conclusions

In this study, we make the micro-temperature sensor to integrate with the gas diffusion layer which is formed by anodization. The temperature of microsensor is measured to range from 20 to 46 °C and its resistance ranges from 1.649 to 1.694 kΩ. Experimental results demonstrate that temperature is almost linearly related to resistance and that accuracy and sensitivity are 0.3 °C and 1.05×10^{-3} °C^{-1}, respectively. This novel method further ensures the feasibility and compatibility of the fabrication process and measurement system used for measuring temperature at all locations in a fuel cell with a bipolar plate of silicon.

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